IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Gattiker et al. DOCKET NO: AUS920030654US1

SERIAL NO.:10/728,172 FILE DATE: `12-03-2003

TITLE OF APPL.: METHOD AND SYSTEM FOR DEFECT EVALUATION USING QUIESCENT POWER PLANE CURRENT (IDDQ) VOLTAGE LINEARITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This information Disclosure Statement is submitted in regards to the above-identified patent application. A PTO-SB/08 form is attached along with copies of the references cited therein.

No fee is believed to be required in connection with this Information Disclosure Statement. However, if there is any fees incurred by this transmittal, please deduct them from IBM Deposit Account No. 09-0447.

Respectfully submitted,

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PTO/SB/08B (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 3

Complete if Known	
Application Number	10/728,172
Filing Date	12-03-2003
First Named Inventor	Gattiker et al.
Art Unit	
Examiner Name	
Attorney Docket Number	AUS920030654US1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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		CHARLES F. HAWKINS AND JERRY M. SODEN Electrical Failure Mode Characterization in CMOS ICs	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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		R. RODRIGUIZ-MONTANES, J.A. SEGURA, V.H.CHAMPAC, J. FIGUERAS, J.A. RUBIO Current vs. Logic Testing of Gate Oxide Short, Floating Gate and Bridging Failures in CMOS, 1991	
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